WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating layer on a silicon substrate;

forming a contact hole on the insulating layer;

forming a silicon layer on the surface of the contact hole; and

forming a selective conductive plug in the contact hole having the silicon layer.

2. The method of manufacturing a semiconductor device according to claim 1, wherein prior to forming the insulating layer, further comprising the steps of:

forming a gate structure on the silicon substrate;

forming an insulating layer on the gate structure; and

forming an oxide layer on the insulating layer of the gate structure.

3. The method of manufacturing a semiconductor device according to claim 2, wherein the oxide layer includes PE-USG oxide layer.

4. The method of manufacturing a semiconductor device according to claim 2, wherein the step of forming the oxide layer on the insulating layer on the gate structure further comprises the steps of:

forming an oxide layer on the insulating layer including the contact hole; and

selectively removing the oxide layer by using a wet etch process.

5. The method of manufacturing a semiconductor device according to claim 3, wherein the PE-USG oxide layer is formed by using SiH_4 as a source gas and by combining N_2O or O_2 therewith.

6. The method of manufacturing a semiconductor device according to claim 5, wherein the PE-USG oxide layer is deposited under the conditions that the flow rate of SiH_4 is between 10 and 200 sccm, that the flowrate of N_2O and O_2 is between 100 and 3000 sccm, the flowrate of He is between 0 and 1000sccm, the pressure is between 0.1 and 50 Torr, the temperature is between 350 and 550℃, and the power is between 100 and 1000W.

7. The method of manufacturing a semiconductor

device according to claim 3, wherein the PE-USG oxide layer has a thickness of between 300 and 1000Å and step coverage is below 50%.

8. The method of manufacturing a semiconductor device according to claim 1, wherein the selectively of the conductive plug is formed by growing a selective single crystal silicon and a selective polycrystalline silicon by using a LPCVD method or a UHVCVD method.

9. The method of manufacturing a semiconductor device according to claim 8, wherein a Si-H-Cl system is first used with the LPCVD method and a DCS-H_2-HCl or MS-H_2-HCl gas system is then used.

10. The method of manufacturing a semiconductor device according to claim 9, wherein the DCS-H_2-HCl gas system is applied under the conditions of temperature between 750 and 950℃, the pressure between 5 and 150Torr, the flow rate of DCS between 0.1 and 1 slm, the flowrate of HCl between 0.1 and 1.0 slm, and the flowrate of H_2 between 30 and 150 slm.

11. The method of manufacturing a semiconductor

device according to claim 9, wherein the MS-H_2-HCl gas system is applied under the conditions of temperature between 750 and 950℃, the pressure between 5 and 150 Torr, the flow rate of MS between 0.1 and 1 slm, the flowrate of HCl between 0.5 and 5.0 slm, and the flowrate of H_2 between 30 and 150 slm.

12. The method of manufacturing a semiconductor device according to claim 2, wherein the insulating layer on the gate structure is a nitride layer.

13. The method of manufacturing a semiconductor device according to claim 4, wherein the oxide layer remains at a thickness of between 200 and 400 Å after the wet etch process.

14. The method of manufacturing a semiconductor device according to claim 1, wherein the silicon layer is a doped amorphous silicon layer.

15. The method of manufacturing a semiconductor device according to claim 14, wherein an in-situ cleaning process is performed prior to forming the amorphous silicon layer.

16. The method of manufacturing a semiconductor device according to claim 15, wherein the in-situ cleaning process is performed by using a RTP process.

17. The method of manufacturing a semiconductor device according to claim 14, wherein the amorphous silicon layer is deposited by using SiH_4 and H_2 gas, and the doping concentration of silicon is between 1 and 2 10^{20} atom/cc.

18. The method of manufacturing a semiconductor device according to claim 14, wherein the amorphous silicon layer is formed on the bottom of the contact hole and side thereof, or only on the side thereof.

19. The method of manufacturing a semiconductor device according to claim 18, wherein the amorphous silicon layer is removed from the resultant structure, except from the bottom of contact hole and the side thereof, by an etch process using HCl and under the conditions that the flow rate of HCl is between 0.1 and 1.0 slm, the flowrate of H_2 is between 1 and 10 slm, the pressure is between 10 and 500 Torr, and the temperature is between 750 and 950℃.

20. The method of manufacturing a semiconductor

device according to claim 1, wherein the silicon layer is an amorphous silicon layer having a thickness of between 50 and 150Å.

21. The method of manufacturing a semiconductor device according to claim 8, wherein the UHVCVD method is applied under the conditions that a H baking process or RTP cleaning process is performed at a temperature of between 850 and 950℃ for 1 to 5 minutes, prior to forming the selective silicon plug.

22. The method of manufacturing a semiconductor device according to claim 8, wherein the selective conductive plug is deposited by using a $SiH_6+Cl_2+H_2$ system under the conditions that the flow rate thereof is between 1 and 10 sccm and up to 20sccm, respectively, using H_2 which includes about 10% PH_3 in-situ at a temperature of between 600 and 800℃ and a pressure of between 1 and 50 Torr.

23. The method of manufacturing a semiconductor device according to claim 1, wherein the selective conductive plug is deposited in an UHV-CVD device for single wafer process and in a tube type UHV-CVD device for SEG.

24. The method of manufacturing a semiconductor device according to claim 23, wherein GeH_4 gas is flowed at a rate of between 0 and 10 sccm in deposition of the selective silicon plug.

25. The method of manufacturing a semiconductor device according to claim 18, wherein the removal of the amorphous silicon layer comprises the steps of removing amorphous silicon layer on the oxide layer and on the bottom of the contact hole by using dry etch process.